REMARKS

This is in response to the Office Action mailed on March 23, 2005, and for which a three-month extension is hereby requested. The Office Action rejected pending claims 68-72 under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. It is respectfully submitted that this rejection is in error and that the claims are fully supported by the present application. Following a discussion of this rejection and the support for the pending claims as provided in the application, the information required under U.S.C. 44.202(a)(1)-(6) is provided.

Rejections under U.S.C. 112, first paragraph

The Office Action rejected pending claims 68-72 under 35 U.S.C. 112, first paragraph, in the first place, stating that for independent claims 68, 71, and 74 "there is no support for the recitation of 'said second group of memory cells being provided for ***storing attribute data*** of said first group of memory cells'", where the emphasis is in the Office Action. It is respectfully submitted that this statement is error and that the full specification provides support for this limitation in multiple locations.

The Office Action itself refers to a first such location in the specification, namely the description of Figure 5 given on page 16, lines 23-35, of the present application. This passage explicitly discloses a first group of memory cells ("data portion" 403) that is provided for storing data and a second group of memory cells ("spare (or shadow) portion 405") that contains header and other data that is closely associated with, and belongs to, the "data portion". Although this passage may use the actual word "attribute", it is clearly describing the "spare portion" as storing, in the plain language meaning of the word, attributes of the "data potion". Thus, the second group of memory cells ("spare (or shadow) portion 405") are storing, in the normal usage of the word, attribute data of the first group of memory cells ("data portion" 403).

A specific example of attribute data is found in independent claims 68 and 74 (but not independent claim 71), namely "wherein said attribute data includes a rewriting number of said first group of memory cells". As discussed in previous responses, U.S. patent number 5,095,344 is incorporated by reference in several location in the specification of the present application and thus forms an integral part of the present application. The specific example of "rewriting

number" as "attribute data" is explicitly and succinctly disclosed at column 28, line 64, to column 29, line 7, patent number 5,095,344:

> The number S of complete erase cyclings experienced by each block is an important information at the system level. If S is known for each block then a block can be replaced automatically with a new redundant block once S reaches $1X10^6$ (or any other set number) of program/erase cycles. S is set at zero initially, and is incremented by one for each complete block erase multiple pulse cycle. ***The value of S at any one time can be stored*** by using for example twenty bits (2^{20} equals approximately $1X10^6$) ***in each block. That way each block carries its own endurance history***.

As the added emphasis indicates, this clearly discloses the example of the number of program/erase cycles, or rewrites, ("S") as attribute data.

The Office Action rejected independent claims 68 and 74 (under 35 U.S.C. 112, first paragraph, in the second place, stating that "there is no support for 'said attribute data includes a ***number of rewriting*** of said first group of memory cells'", where the emphasis is in the Office Action. (This limitation is not found in independent claim 71.) It is respectfully submitted that this statement is also error and that support for this limitation as well.

The Office Action appears to base this particular rejection on the basis that the quantity "S", discussed above, is "**a number of full erase cycles and is not related to** '*a number of rewriting of a first group of memory cells*'", where the emphasis is from the Office Action. The second part of this statement is incorrect: S is the number of erase cycles, but *it is also the number of rewrites*. This is again explicitly disclosed in the passage of of patent number 5,095,344 quoted above:

> The number S of complete erase cyclings experienced by each block is an important information at the system level. If S is known for each block then a block can be replaced automatically with a new redundant block once S reaches $1X10^6$ (or any other set number) of ***program/erase cycles***. S is set at zero initially, and is incremented by one for each complete block erase multiple pulse cycle.

The exemplary embodiments of the present invention are flash memories. It is basic to the operation of such memories that a rewrite always includes a preceding erase. As the added emphasis show, the quantity "S" is the number of "*program/erase cycles*" and thus corresponds to the "rewrite number" of the first group of memory cells.

For theses reasons, it is respectfully submitted that the rejection of claims 68-72 under 35 U.S.C. 112, first paragraph, is not well founded and should be withdrawn.

U.S.C. 44.202(a)(1)-(6)

The present application contains a number of inventions, including those noted in the first paragraph of the Office Action's conclusion. Another of the inventions of the present application is that to which the pending claims, copied from U.S. patent 5,818,754, are drawn. Much of the following has previously bee presented in the Request for Declaration of an Interference originally filed on March 17, 2000.

Consequently, in response to the various portions of 37 CFR §41.202(a):

(1) Identification of Patent

Section (1) requires sufficient information to identify the patent with which an interference is sought. Independent claims 68 and 74 of the present application are respectively exact copies of claims 7 and 18 of U.S. patent number 5,818,754, of Ogura, issued October 6, 1998. Independent claim 71 of the present application is an exact copy of claims 12 of U.S. patent number 5,818,754, of Ogura, issued October 6, 1998, except that the last word "bits" of the claim has been changed to bytes.

(2) Identification of Claims Believed to Interfere, ProposedCount, and Claim Correspondence

Claim 68 is an exact copy of claim 7 of U.S. patent number 5,818,754, and, consequently, so corresponds.

Claim 69 is closely based upon claim 8 of U.S. patent number 5,818,754, and so corresponds.

Claim 70 is closely based upon claim 11 of U.S. patent number 5,818,754, and so corresponds.

Claim 71 is closely based upon claim 12 of U.S. patent number 5,818,754, and so corresponds.

Claim 72 is closely based upon claim 15 of U.S. patent number 5,818,754, and so corresponds.

Claim 74 is an exact copy of claim 18 of U.S. patent number 5,818,754, and, consequently, so corresponds.

Claim 68 of the present application, which is an exact copy of claim 7 of U.S. patent number 5,818,754, is suggested as Count 1:

Count 1

A memory comprising:
a plurality of word lines;
a plurality of bit lines; and
a plurality of memory cells, wherein each of said memory cells corresponds to a selected one of said plurality of word lines and a selected one of said plurality of bit lines;
wherein said plurality of memory cells are divided into a first group of memory cells and a second group of memory cells, said first group of memory cells being provided for storing data and said second group of memory cells being provided for storing attribute data of said first group of memory cells, wherein said attribute data includes a number of rewriting of said first group of memory cells.

As claim 68 of the present application, which is an exact copy of claim 7 of U.S. patent number 5,818,754, is also a direct copy of the proposed Count 1, they so correspond.

Claim 69 of the present application, which is closely based upon claim 8 of U.S. patent number 5,818,754, is suggested as Count 2:

Count 2

A memory as claimed in claim 68, wherein said first group of memory cells and said second group of memory cells are accessible by a common sector address.

As claim 69 of the present application is a direct copy of the proposed Count 2, it so corresponds. As claim 8 of U.S. patent number 5,818,754 differs only in that is specifies "a same address" instead of "a common sector address", it also corresponds.

Claim 70 of the present application, which is closely based upon claim 11 of U.S. patent number 5,818,754, is suggested as Count 3:

Count 3

A memory as claimed in claim 68, further comprising an erasing circuit to erase data stored in at least one or more of said plurality of memory cells in response to an erasing signal.

As claim 70 of the present application is a direct copy of the proposed Count 3, it so corresponds. As claim 11 of U.S. patent number 5,818,754 differs only in that is specifies "erase content data" instead of "erase data", it also corresponds.

Claim 71 of the present application, which is closely based upon claim 12 of U.S. patent number 5,818,754, is suggested as Count 4:

Count 4

A memory including a plurality of memory cell blocks, each of said plurality of memory cell blocks comprising:

a plurality of word lines;

a plurality of bit lines; and

a plurality of memory cells, each of said plurality of memory cells being connected between one of said word lines and one of said bit lines;

wherein said plurality of memory cells are divided into a first group of memory cells and a second group of memory cells, wherein said first group of memory cells are provided for storing data and said second group of memory cells are provided for storing attribute data of said first group of memory cells, and wherein said first group of memory cells are memory cells storing 512 bytes.

As claim 71 of the present application is a direct copy of the proposed Count 4, it so corresponds. As claim 12 of U.S. patent number 5,818,754 differs only in that is specifies "512 bits" instead of "512 bytes", it also corresponds.

Claim 72 of the present application, which is closely based upon claim 15 of U.S. patent number 5,818,754, is suggested as Count 5:

Count 5

The memory as claimed in claim 71, further comprising an erasing circuit to erase contents of all of said plurality of memory cells in response to an erasing signal.

As claim 72 of the present application is a direct copy of the proposed Count 5, it so corresponds. As claim 15 of U.S. patent number 5,818,754 differs only in that is specifies "said all memory cells of a selected one of said memory blocks, selected by an address signal" instead of "all of said plurality of memory cells", it also corresponds.

Claim 74 of the present application, which is an exact copy of claim 18 of U.S. patent number 5,818,754, is suggested as Count 6:

Count 6

A memory comprising:
a plurality of word lines;
a plurality of bit lines; and
a plurality of memory cells, wherein each of said memory cells corresponds to a selected one of said plurality of word lines and a selected one of said plurality of bit lines;
A memory comprising:
a plurality of memory cell blocks further comprising;
a plurality of word lines;
a plurality of bit lines; and
a plurality of memory cells, wherein each of said plurality of memory cells corresponds to a selected one of said word lines and a selected one of said bit lines; and wherein said plurality of memory cells are divided into a first group of memory cells and a second group of memory cells, said first group of memory cells provided for storing data and said second group of memory cells provided for storing attribute data of said first group of memory cells, and wherein said attribute data includes a rewriting number of said first group of memory cells.

As claim 74 of the present application, which is an exact copy of claim 18 of U.S. patent number 5,818,754, is also a direct copy of the proposed Count 1, they so correspond.

(3) Claim Chart for the Counts

As the proposed Count 1 is both Claim 68 of the present application and an exact copy of claim 7 of U.S. patent number 5,818,754, they correspond exactly:

Claim 68 of Present Application	Count 1
A memory comprising: a plurality of word lines;	A memory comprising: a plurality of word lines;
a plurality of bit lines; and	a plurality of bit lines; and
a plurality of memory cells, wherein each of said memory cells corresponds to a selected one of said plurality of word lines and a selected one of said plurality of bit lines;	a plurality of memory cells, wherein each of said memory cells corresponds to a selected one of said plurality of word lines and a selected one of said plurality of bit lines;
wherein said plurality of memory cells	wherein said plurality of memory cells

are divided into a first group of memory cells and a second group of memory cells, said first group of memory cells being provided for storing data and said second group of memory cells being provided for storing attribute data of said first group of memory cells, wherein said attribute data includes a number of rewriting of said first group of memory cells.	are divided into a first group of memory cells and a second group of memory cells, said first group of memory cells being provided for storing data and said second group of memory cells being provided for storing attribute data of said first group of memory cells, wherein said attribute data includes a number of rewriting of said first group of memory cells.

Claim 7 of U.S. patent number 5,818,754	Count 1
A memory comprising: a plurality of word lines;	A memory comprising: a plurality of word lines;
a plurality of bit lines; and	a plurality of bit lines; and
a plurality of memory cells, wherein each of said memory cells corresponds to a selected one of said plurality of word lines and a selected one of said plurality of bit lines;	a plurality of memory cells, wherein each of said memory cells corresponds to a selected one of said plurality of word lines and a selected one of said plurality of bit lines;
wherein said plurality of memory cells are divided into a first group of memory cells and a second group of memory cells, said first group of memory cells being provided for storing data and said second group of memory cells being provided for storing attribute data of said first group of memory cells, wherein said attribute data includes a number of rewriting of said first group of memory cells.	wherein said plurality of memory cells are divided into a first group of memory cells and a second group of memory cells, said first group of memory cells being provided for storing data and said second group of memory cells being provided for storing attribute data of said first group of memory cells, wherein said attribute data includes a number of rewriting of said first group of memory cells.

As the claims are identical and the present application will prevail on priority, as described in the next section, the claims interfere within the meaning of Sec. 41.203(a).

As the proposed Count 2 is Claim 69 of the present application, they correspond exactly:

Claim 69 of Present Application	Count 2
A memory as claimed in claim 68, wherein said first group of memory cells and said second group of memory cells are accessible by a common sector address.	A memory as claimed in claim 68, wherein said first group of memory cells and said second group of memory cells are accessible by a common sector address.

As claim 8 of U.S. patent number 5,818,754 differs only in that is specifies specifies "erase content data" instead of "erase data", it is not patentably distinct and also corresponds to count 2:

Claim 8 of U.S. patent number 5,818,754	Count 2
A memory as claimed in claim 7, wherein said first group of memory cells and said second group of memory cells are accessible by a same address.	A memory as claimed in claim 68, wherein said first group of memory cells and said second group of memory cells are accessible by a common sector address.

(The proposed Count 1 is both Claim 68 of the present application and an exact copy of claim 7 of U.S. patent number 5,818,754.) As the claims correspond and the present application will prevail on priority, as described in the next section, the claims interfere within the meaning of Sec. 41.203(a).

As the proposed Count 3 is Claim 70 of the present application, they correspond exactly:

Claim 70 of Present Application	Count 3
A memory as claimed in claim 68, further comprising an erasing circuit to erase data stored in at least one or more of said plurality of memory cells in response to an erasing signal.	A memory as claimed in claim 68, further comprising an erasing circuit to erase data stored in at least one or more of said plurality of memory cells in response to an erasing signal.

As claim 11 of U.S. patent number 5,818,754 differs only in that is specifies "erase content data" instead of "erase data", it is not patentably distinct and also corresponds to count 3:

Claim 11 of U.S. patent number 5,818,754	Count 3
A memory as claimed in claim 7, further comprising an erasing circuit to erase	A memory as claimed in claim 68, further comprising an erasing circuit to erase

content data stored in at least one or more of said plurality of memory cells in response to an erasing signal.	data stored in at least one or more of said plurality of memory cells in response to an erasing signal.

(The proposed Count 1 is both Claim 68 of the present application and an exact copy of claim 7 of U.S. patent number 5,818,754.) As the claims correspond and the present application will prevail on priority, as described in the next section, the claims interfere within the meaning of Sec. 41.203(a).

As the proposed Count 4 is Claim 71 of the present application, they correspond exactly:

Claim 71 of Present Application	Count 4
A memory including a plurality of memory cell blocks, each of said plurality of memory cell blocks comprising: a plurality of word lines;	A memory including a plurality of memory cell blocks, each of said plurality of memory cell blocks comprising: a plurality of word lines;
a plurality of bit lines; and	a plurality of bit lines; and
a plurality of memory cells, each of said plurality of memory cells being connected between one of said word lines and one of said bit lines;	a plurality of memory cells, each of said plurality of memory cells being connected between one of said word lines and one of said bit lines;
wherein said plurality of memory cells are divided into a first group of memory cells and a second group of memory cells, wherein said first group of memory cells are provided for storing data and said second group of memory cells are provided for storing attribute data of said first group of memory cells, and wherein said first group of memory cells are memory cells storing 512 bytes.	wherein said plurality of memory cells are divided into a first group of memory cells and a second group of memory cells, wherein said first group of memory cells are provided for storing data and said second group of memory cells are provided for storing attribute data of said first group of memory cells, and wherein said first group of memory cells are memory cells storing 512 bytes.

As claim 12 of U.S. patent number 5,818,754 differs only in that is specifies "512 bits" instead of "512 bytes", it is not patentably distinct and also corresponds to count 4:

Claim 12 of U.S. patent number 5,818,754	Count 4
A memory including a plurality of memory cell blocks, each of said plurality of memory cell blocks comprising: a plurality of word lines;	A memory including a plurality of memory cell blocks, each of said plurality of memory cell blocks comprising: a plurality of word lines;
a plurality of bit lines; and	a plurality of bit lines; and
a plurality of memory cells, each of said plurality of memory cells being connected between one of said word lines and one of said bit lines;	a plurality of memory cells, each of said plurality of memory cells being connected between one of said word lines and one of said bit lines;
wherein said plurality of memory cells are divided into a first group of memory cells and a second group of memory cells, wherein said first group of memory cells are provided for storing data and said second group of memory cells are provided for storing attribute data of said first group of memory cells, and wherein said first group of memory cells are memory cells storing 512 bits.	wherein said plurality of memory cells are divided into a first group of memory cells and a second group of memory cells, wherein said first group of memory cells are provided for storing data and said second group of memory cells are provided for storing attribute data of said first group of memory cells, and wherein said first group of memory cells are memory cells storing 512 bytes.
As the claims correspond and the present application will prevail on priority, as described in the next section, the claims interfere within the meaning of Sec. 41.203(a). As the proposed Count 5 is Claim 72 of the present application, they correspond exactly:	

Claim 72 of Present Application	Count 5
The memory as claimed in claim 71, further comprising an erasing circuit to erase contents of all of said plurality of memory cells in response to an erasing signal.	The memory as claimed in claim 71, further comprising an erasing circuit to erase contents of all of said plurality of memory cells in response to an erasing signal.

As claim 15 of U.S. patent number 5,818,754 differs only in that is specifies "said all memory cells of a selected one of said memory blocks, selected by an address signal" instead of

"all of said plurality of memory cells", it is not patentably distinct and also corresponds to count 5:

Claim 11 of U.S. patent number 5,818,754	Count 5
The memory as claimed in claim 12 , further comprising an erasing circuit to erase contents of said all memory cells of a selected one of said memory blocks, selected by an address signal in response to an erasing signal.	The memory as claimed in claim 71, further comprising an erasing circuit to erase contents of all of said plurality of memory cells in response to an erasing signal.

(The proposed Count 4 is both Claim 71 of the present application and corresponds to claim 12 of U.S. patent number 5,818,754.) As the claims correspond and the present application will prevail on priority, as described in the next section, the claims interfere within the meaning of Sec. 41.203(a).

As the proposed Count 6 is both Claim 74 of the present application and an exact copy of claim 18 of U.S. patent number 5,818,754, they correspond exactly:

Claim 74 of Present Application	Count 6
A memory comprising: a plurality of memory cell blocks further comprising;	A memory comprising: a plurality of memory cell blocks further comprising;
a plurality of word lines;	a plurality of word lines;
a plurality of bit lines; and	a plurality of bit lines; and
a plurality of memory cells, wherein each of said plurality of memory cells corresponds to a selected one of said word lines and a selected one of said bit lines; and wherein said plurality of memory cells are divided into a first group of memory cells and a second group of memory cells, said first group of memory cells provided for storing data and said second group of memory cells	a plurality of memory cells, wherein each of said plurality of memory cells corresponds to a selected one of said word lines and a selected one of said bit lines; and wherein said plurality of memory cells are divided into a first group of memory cells and a second group of memory cells, said first group of memory cells provided for storing data and said second group of memory cells

provided for storing attribute data of said first group of memory cells, and wherein said attribute data includes a rewriting number of said first group of memory cells.	provided for storing attribute data of said first group of memory cells, and wherein said attribute data includes a rewriting number of said first group of memory cells.

Claim 18 of U.S. patent number 5,818,754	Count 6
A memory comprising: a plurality of memory cell blocks further comprising;	A memory comprising: a plurality of memory cell blocks further comprising;
a plurality of word lines;	a plurality of word lines;
a plurality of bit lines; and	a plurality of bit lines; and
a plurality of memory cells, wherein each of said plurality of memory cells corresponds to a selected one of said word lines and a selected one of said bit lines; and wherein said plurality of memory cells are divided into a first group of memory cells and a second group of memory cells, said first group of memory cells provided for storing data and said second group of memory cells provided for storing attribute data of said first group of memory cells, and wherein said attribute data includes a rewriting number of said first group of memory cells.	a plurality of memory cells, wherein each of said plurality of memory cells corresponds to a selected one of said word lines and a selected one of said bit lines; and wherein said plurality of memory cells are divided into a first group of memory cells and a second group of memory cells, said first group of memory cells provided for storing data and said second group of memory cells provided for storing attribute data of said first group of memory cells, and wherein said attribute data includes a rewriting number of said first group of memory cells.

As the claims are identical and the present application will prevail on priority, as described in the next section, the claims interfere within the meaning of Sec. 41.203(a).

(4) How Applicant Will prevail on Priority

As specified in the "Cross-Reference to Related Application" section aedded by the Preliminary Amendment filed on August 28, 1998, to the beginning of the application of which

the present application is a continued prosecution application, the present application is entitled to an effective filed date of April 13, 1989, due to the benefit of:

U.S. Ser. No. 08/771, 708, filed December 20, 1996, now patent number 5,991,517,

U.S. Ser. No. 08/174,768, filed December 29, 1993, now patent number 5,602,987,

U.S. Ser. No. 07/963,838, filed October 20, 1992, now patent number 5,297,148,

U.S. Ser. No. 07/337,566, filed April 13, 1989.

U.S. patent number 5,818,754 has an United States filing date of December 27, 1996, claiming priority from a Japanese patent application with a date of December 27, 1995, over six years after the priority date to which the present application is entitled.

(5,6) Claim Charts

The following claim charts are for the pending claims that interfere. They show the corresponding written description for each claim in the specification of the present application. They also show where the disclosure provides a constructive reduction to practice within the scope of the interfering subject matter.

More specifically:

68. A memory comprising: a plurality of word lines; a plurality of bit lines; and a plurality of memory cells, wherein each of said memory cells corresponds to a selected one of said plurality of word lines and a selected one of said plurality of bit lines;	Figures 15a and 15b of US patent number 5,095,344 (`344) show such a memory, with each cell corresponding to a selected one of the rows (word lines) and a selected one of the columns (bit lines). The structure is discussed more in section VIII of the `344 patent beginning at column 32, line 57.
wherein said plurality of memory cells are divided into a first group of memory cells and a second group of memory cells, said first group of memory cells being provided for storing data and said second group of memory cells being provided for storing attribute data	Note that this limitation is discussed in more detail above, in relation to the rejections under U.S.C. 112, first paragraph. Figure 5 of the present application, described beginning at page 16, line 23

of said first group of memory cells, wherein said attribute data includes a number of rewriting of said first group of memory cells.	describes such a division into portions 403 and 405. Figure 12 of `344 and its description beginning at column 28, line 36 describes storing in an individual block the number S of program/erase cycles: "The value of S at any one time can be stored ... in each block. That way each block carries its own endurance history."(`344, col. 29, lns.3-7)
69. A memory as claimed in claim 68, wherein said first group of memory cells and said second group of memory cells are accessible by a common sector address.	On accessing by a common sector address in, for example, a read process, see page 18, lines 4-6, of the present application
70. A memory as claimed in claim 68, further comprising an erasing circuit to erase data stored in at least one or more of said plurality of memory cells in response to an erasing signal.	Figures 3A and 3B of the present application, whose description begins on lined 30 of page 9, present erase select circuits.

71. A memory including a plurality of memory cell blocks, each of said plurality of memory cell blocks comprising: a plurality of word lines; a plurality of bit lines; and a plurality of memory cells, each of said plurality of memory cells being connected between one of said word lines and one of said bit lines;	Figures 15a and 15b of US patent number 5,095,344 (`344) show such a memory, with each cell corresponding to a selected one of the rows (word lines) and a selected one of the columns (bit lines). The structure is discussed more in section VIII of the `344 patent beginning at column 32, line 57.
wherein said plurality of memory cells are divided into a first group of memory cells and a second group of memory cells, wherein said first group of memory cells are provided for storing data and said second group of memory cells are provided for storing attribute data of said first group of memory cells, and wherein said first group of memory cells are memory cells storing 512 bytes.	Note that this limitation is discussed in more detail above, in relation to the rejections under U.S.C. 112, first paragraph. Figure 5 of the present application, described beginning at page 16, line 23 describes such a division into portions 403 and 405. Figure 12 of `344 and its description beginning at column 28, line 36 describes storing in an individual block the example of the number S of program/erase cycles: "The value of S at any one time can be stored ... in each block. That way each block carries its own endurance history."(`344, col. 29, lns.3-7) On storing 512 bytes, see, for example, page 9, line 19, of the present application.

72. The memory as claimed in claim 71, further comprising an erasing circuit to erase contents of all of said plurality of memory cells in response to an erasing signal.	Figures 3A and 3B of the present application, whose description begins on lined 30 of page 9, present erase select circuits.
74. A memory comprising: a plurality of memory cell blocks further comprising; a plurality of word lines; a plurality of bit lines; and	Figures 15a and 15b of US patent number 5,095,344 (`344) show such a memory, with each cell corresponding to a selected one of the rows (word lines) and a selected one of the columns (bit lines). The structure is discussed more in section VIII of the `344 patent beginning at column 32, line 57.
a plurality of memory cells, wherein each of said plurality of memory cells corresponds to a selected one of said word lines and a selected one of said bit lines; and wherein said plurality of memory cells are divided into a first group of memory cells and a second group of memory cells, said first group of memory cells provided for storing data and said second group of memory cells provided for storing attribute data of said first group of memory cells, and wherein said attribute data includes a rewriting number of said first group of memory cells.	Figures 15a and 15b of `344 show a plurality of memory cells each corresponding to a selected one of the rows and a selected one of the columns. Note that the "storing attribute data" limitation is discussed in more detail above, in relation to the rejections under U.S.C. 112, first paragraph. Figure 5 of the present application, described beginning at page 16, line 23 describes such a division into portions 403 and 405. Figure 12 of `344 and its description beginning at column 28, line 36 describes storing in an individual block the number S of program/erase cycles: "The value of S at any one time can be stored ...

	in each block. That way each block carries its own endurance history."(`344, col. 29, lns.3-7)

As presented above, it is respectfully submitted that the present application supports all of the currently pending claims and an early indication of their allowability is earnestly solicited. In the meantime, a phone call to the undersigned is invited should there be any questions.

Respectfully submitted,

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9/19/05
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